Claims

What is claimed is:

1. A method of synchronous reading for a plurality of words in a memory system, comprising:

selecting said plurality of words to be read, said plurality of words having a first group of words and at least one subsequent group of words;

reading said plurality of words into a plurality of data registers during a clock latency period; and

shifting out said plurality of words synchronously at the end of said latency period.

2. The method of claim 1, wherein said step of reading further comprises the following steps:

determining from said plurality of words which said first group of words is to be read, said first group of words having a first tier and a subsequent tier;

reading said first tier of said first group of words into said plurality of data registers at the beginning of said latency period;

deleting said first tier of said first group of words from said plurality of data registers after said reading step during said latency period;

loading said first tier of said subsequent group of words into said plurality of data registers after said step of deleting during said latency period; and

reading said subsequent tier of said first group of words into said plurality of data registers after said step of loading during said latency period.

3. The method of claim 2, wherein the step of determining which said first group of words to be read further comprises:

checking whether an address field of said first group of words to be read belongs to a first address field or a subsequent address field, if said address field of said first group of words belongs to said first address field then

selecting said first tier of words whose address coincides with an initial address of said first tier of words; otherwise

selecting said first group of words whose address coincides with an initial address of subsequent tier of words.

4. The method of claim 2, wherein the step of reading said first tier of said first group of words further comprises checking whether a last bit of said first tier of words has been reached, if said last bit of said first tier of words has not been reached, continuing reading; otherwise

continuing to read said subsequent tier of words.

5. A two-tier column decoder to facilitate synchronous reading of a plurality of words in a memory system, comprising:

a sub bitline decoder coupled to a main bit line of said memory system for decoding a most significant bit of said plurality of words to be read and

for determining whether an address of said plurality of words is in an low or high order word;

a first tier decoder coupled to said sub bit line decoder to select both said even and odd addresses of said plurality of words for a first reading during a clock latency period; and

a second tier decoder coupled to said first tier decoder to select either said lower or higher word addresses for a subsequent reading.

6. The two-tier column decoder of claim 5, wherein said second tier decoder further comprises:

an array of decoder blocks coupled to one another, each having a plurality of input terminals, an output terminal, and a feedback terminal for determining whether said plurality of words is said lower or higher or both.

7. The two-tier column decoder system of claim 6, wherein each decoder block further comprises:

a first NOR logic gate adapted to receive said plurality of input terminals;

a second NOR logic gate adapted to receive an output of said first NOR logic gate; and

a plurality of transistors coupled together to receive a feedback signal from a subsequent decoder block and coupled to said second NOR logic gate.

8. A two-tier column decoder to facilitate synchronous reading a plurality of words in a memory system, comprising:

a most-significant-bit decoding means for decoding a most significant bit of said plurality of words to be read and determining whether an address of said plurality of words is in an lower or an higher address, said means being coupled to a main bit line of said memory system;

a first selecting means for selecting both said even and odd addresses for a first reading during a clock latency period, said selecting means coupled to said first means; and

a second selecting means coupled to said second means for selecting either even or odd address for a subsequent reading.

9. The two-tier column decoder of claim 8, wherein said third decoding means further comprises:

a plurality of decoding means coupled to one another, each having a plurality of input terminals, an output terminal, and a feedback terminal for determining whether said plurality of words is either said odd or even address.

10. The two-tier column decoder of claim 9, wherein each decoding means further comprises:

a first logic means adapted to receive said plurality of input terminals for producing a status signal of said plurality of input signals;

a second logic means adapted to receive said status signal for producing a signal that determines

whether said plurality of input terminals are in said even or odd address;

a plurality of transistor feedback means adapted to receive a feedback output signal from a subsequent decoding means and coupled to said second logic means for providing a status of said subsequent decoding means.

11. A burst mode operation system for fast synchronous reading in a memory system, comprising:

a burst controller adapted to receive an input clock signal, a variable latency signal, and a burst sequence control signal from said memory system to produce a plurality of words to be read and an output clock signal;

an address controller coupled to said burst controller for producing addresses of said plurality of words to be read;

a two-tier column decoder adapted to receive said addresses from said address controller for producing a first tier address and a second tier address; and

a row decoder adapted to receive said addresses from said address controller for producing row addresses of said plurality of words to be read.

12. The burst mode operation system of claim 11, wherein said burst controller further comprises:

a clock driver adapted to receive said input clock signal to produce an internal and an external clock signal;

a burst control and ready generator adapted to receive said internal clock signal, said external clock

signal for producing said output clock signal and a page boundary signal;

a word counter coupled to said output clock signal for producing a plurality of word address counts;

a burst sequence control adapted to receive one of said plurality of word address counts and said output clock signal for producing a plurality of read signals; and

a word generator coupled to said word counter and a word output controller for producing said plurality of words to be read.

13. The burst mode operation system of claim 11, wherein said address controller further comprises:

a burst control clock device adapted to receive said output clock signal, said plurality of word address counts to produce at least one burst control clock signal;

a Y-address register and counter adapted to receive said output clock signal and said addresses of said plurality of words;

an end of page detector adapted to receive a plurality of address counter signals from said Y-address register and counter to produce an end of page signal;

an X-address clock adapted to receive said end of page signal to produce an X-clock signal; and

an X-address register and counter adapted to receive said X-clock signal, and addresses of said plurality of words to be read.